Introduction to System IC and Design Flow
Outline

- System-on-a-Chip (SoC) Trend
- SoC Integration & Challenge
- System-in-a-Package (SIP)
- IC Industry and Chip Production Flow
- System IC Design Flow
- Chip Debugging Tools and Reliability Issues
SoC Concept

System on a Board

System on a Chip
Soc Advantages

- Minimize System Cost
  - PCB, passive components
  - Assembling
  - Testing

- Compact System Size
  - Board layout vs. chip layout

- Reduce System Power Consumption
  - I/O, passive components, current levels

- Increase System Performance
  - Interconnecting delay
  - High speed parallel bus
## Years 2002 – 2008 Worldwide Communication SoC Market Values

Unit: Million U.S. Dollars

<table>
<thead>
<tr>
<th>Product</th>
<th>2002</th>
<th>2003</th>
<th>2004</th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
<th>2008</th>
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<tr>
<td>Digital Cellular</td>
<td>7,480</td>
<td>9,463</td>
<td>12,560</td>
<td>15,210</td>
<td>15,855</td>
<td>17,202</td>
<td>19,013</td>
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<td>LAN Wireless</td>
<td>138</td>
<td>333</td>
<td>492</td>
<td>662</td>
<td>777</td>
<td>938</td>
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<tr>
<td>Mobile Infrastructure</td>
<td>325</td>
<td>344</td>
<td>418</td>
<td>537</td>
<td>511</td>
<td>479</td>
<td>481</td>
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<tr>
<td>Other Mobile Comms.</td>
<td>378</td>
<td>520</td>
<td>673</td>
<td>859</td>
<td>1,077</td>
<td>1,215</td>
<td>1,440</td>
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<tr>
<td>LAN</td>
<td>140</td>
<td>184</td>
<td>248</td>
<td>316</td>
<td>348</td>
<td>392</td>
<td>446</td>
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<tr>
<td>Premises and CO Line Card</td>
<td>167</td>
<td>161</td>
<td>188</td>
<td>201</td>
<td>199</td>
<td>204</td>
<td>219</td>
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<tr>
<td>Broadband Remote Access</td>
<td>918</td>
<td>1,313</td>
<td>1,617</td>
<td>1,793</td>
<td>1,717</td>
<td>1,837</td>
<td>1,978</td>
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<tr>
<td>Public Infrastructure</td>
<td>304</td>
<td>360</td>
<td>481</td>
<td>607</td>
<td>667</td>
<td>810</td>
<td>934</td>
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<tr>
<td>Other Wired Comms.</td>
<td>428</td>
<td>568</td>
<td>811</td>
<td>1,128</td>
<td>1,175</td>
<td>1,365</td>
<td>1,515</td>
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<tr>
<td>Total Communications</td>
<td>10,278</td>
<td>13,246</td>
<td>17,488</td>
<td>21,313</td>
<td>22,326</td>
<td>24,442</td>
<td>27,160</td>
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</table>

Source: Dataquest (2004/06)
Example 1: Siemens C35i Phone

1. Infineon E-GOLD PMB2851E, GSM Baseband controller and DSP.
2. 32.768kHz crystal
3. NIY
4. Bottom connector
5. FLASH
6. Power supply IC
7. VCO
8. Epcoc B4846; SAW filter, 225.0MHz
9. PCB pads to Battery
10. 13MHz crystal
11. Tx VCO
12. Hitachi PF08112B; Power amplifier
14. Diplex filter
15. NIY
16. Epcos B4127 SAW filter 942.5MHz
17. NIY
18. PCB pads to SIM card holder
19. Synthesizer (?)
20. Hitachi HD155124F– Bright II; GSM Transceiver Circuit
21. Infineon PMB2906: Analog interface IC (E-GAIM). Interfaces analogue signals (I/Q, voiceband, PA-control, charging control signals) to the digital domain
Example 2: Philips DAB Receiver

Integration vs. Diversity & Process
System Integration Trend - Cfone

~2000

RF/IF
- Transistors
- Diodes
- Synthesizer IC
- Frequency Converter
- LNA
- RF Switch
- VCOs
- Filters
- PA

Baseband
- CPU/DSP
- Audio Processor
- Memories
- Power Management
- A/D
- D/A

Passive
- Resistors
- Inductors
- Capacitors

Source: 工研院經資中心ITIS計畫(2002/10)
TI-DRP GSM cellular phone solution

- Power Amplifier
- RF Codec
  ADC and DAC
- Digital Baseband
- Transceiver
- Frequency Synthesizer
- Memory
- Power Management

- Power Amplifier
- Digital and RF SOC
- Memory
- Power Management

½ Board size
½ Power
½ Silicon Area
Outline

- System-on-a-Chip (SoC) Trend
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Affecting Factors for System Integration

- **Process Migration**
  - Faster digital to implement RF
  - Density & Yield improving

- **IP Resources**
  - Reusable IP
  - Cooperation or Merge

- **EDA Tools Support**
  - System Integration Tools
  - System Verification Tools
## Histories of Key IC Components

<table>
<thead>
<tr>
<th>Logic</th>
<th>1st Bipolar Transistor</th>
<th>Belllab in 1956</th>
<th>Memory</th>
<th>1st integrated memory-cell</th>
<th>NEC in 1966</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1st Bipolar ECL</td>
<td>IBM in 1957</td>
<td></td>
<td>1st 1Kb 3T MOS DRAM</td>
<td>Intel/Honeywell in 1970</td>
</tr>
<tr>
<td></td>
<td>1st IC</td>
<td>Fairchild in 1960</td>
<td></td>
<td>1st 2Kb EPROM</td>
<td>Intel in 1971</td>
</tr>
<tr>
<td></td>
<td>1st TTL</td>
<td>Fairchild in 1962</td>
<td></td>
<td>1st 1T DRAM</td>
<td>Siemens in 1972</td>
</tr>
<tr>
<td></td>
<td>1st CMOS</td>
<td>Fairchild in 1963</td>
<td></td>
<td>1st mux-addressed 16Kb DRAM</td>
<td>Mostek in 1977</td>
</tr>
<tr>
<td></td>
<td>1st 4-bit NMOS uP</td>
<td>Intel in 1974</td>
<td></td>
<td>1st 4Kb pseudo-SRAM</td>
<td>Intel in 1979</td>
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<tr>
<td></td>
<td>1st 32-bit CMOS uP</td>
<td>Belllab in 1981</td>
<td></td>
<td>1st 16Kb EEPROM</td>
<td>Intel in 1980</td>
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<tr>
<td></td>
<td>1st 32-bit RISC uP</td>
<td>Standford+Berkeley in 1984</td>
<td></td>
<td>1st 256Kb Flash</td>
<td>Toshiba in 1985</td>
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<tr>
<td></td>
<td>1st 100MHz CMOS uP</td>
<td>Intel in 1991</td>
<td></td>
<td>1st 256b FRAM</td>
<td>Ramtron in 1988</td>
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<tr>
<td></td>
<td>1st 64-bit CMOS uP-200MHz</td>
<td>DEC in 1992</td>
<td></td>
<td>1st multi-level 32Mb Flash</td>
<td>Intel in 1995</td>
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<tr>
<td></td>
<td>1st 32-bit 1Ghz uP-0.18u</td>
<td>Intel in 2000</td>
<td></td>
<td>1st analog shift-register</td>
<td>Philips in 1972</td>
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<tr>
<td>DSP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analog</td>
<td>1st PLL IC</td>
<td>Signetics in 1969</td>
<td></td>
<td>1st switched-capacitor Filter</td>
<td>Berkeley in 1978</td>
</tr>
<tr>
<td></td>
<td>1st MOS voice-encoder</td>
<td>Berkeley in 1976</td>
<td></td>
<td>1st DSP</td>
<td>Belllab in 1980</td>
</tr>
<tr>
<td></td>
<td>1st switch-capacitor Filter</td>
<td>Berkeley in 1977</td>
<td></td>
<td>1st floating-point 32-bit DSP</td>
<td>Belllab in 1985</td>
</tr>
<tr>
<td></td>
<td>1st echo-canceller</td>
<td>Belllab in 1983</td>
<td></td>
<td>1st Video DSP</td>
<td>NEC in 1987</td>
</tr>
<tr>
<td></td>
<td>1st 1-chip Pager</td>
<td>Philips in 1991</td>
<td></td>
<td>1st CMOS read-channel</td>
<td>Hitachi in 1993</td>
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<tr>
<td></td>
<td>1st GSM Transceiver</td>
<td>Belllab in 1995</td>
<td></td>
<td>1st low-power 16-bit DSP</td>
<td>Matsushida in 1993</td>
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<tr>
<td></td>
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<td>1st 1024-QAM cable-mode DSP</td>
<td>Broadcom in 1998</td>
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<tr>
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<td></td>
<td></td>
<td>1st 5Ghz OFDM-BB 80Mb/s</td>
<td>Imec in 2000</td>
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</tbody>
</table>

Source: ISSCC 50th years
Moore’s Law and Extensions

Gordon Moore (ISSCC2003):
- Moore’s Law will extend another 10-15 years.
- But no exponential is forever, so delayed Moore’s Law (valid in the past 50 years) will be more realistic for the next 10-15 years.

Source: Intel
Technology Migration

TSMC Logic Technology Roadmap

Available Technologies 2004 2005 2006

Low Power
- CL018LP
- CL015LP
- CL013LP

CLN90LP 1.2V/2.5V
CLN90LP 1.2V/3.3V
CLN65LP

High Speed
- CL018LV
- CL015LV
- CL013LV

CL013LV(LK)
CLN011LV 1.2V/1.8, 2.5, 3.3V
CLN90GT 1.2V/2.5V
CLN90GT 1.2V/1.8V
CLN65HS

General Purpose
- 1.2~0.15um
- CL013G 1.2V/2.5, 3.3V
- 1.2V/2.5, 3.3V
- CLN90G 1.0V/2.5V
- CLN90G 1.0V/1.8, 3.3V

CLN90G 1.0V/2.5V
CLN90G 1.0V/1.8, 3.3V
CLN65G

Source: TSMC Technology Roadmap (Fall 2004)
IP Resources

- IP Libraries (in-company)

- IP Providers
  - Faraday, Global UniChip, PGC, FameG, …
  - Artisan, ARM, MIPS, Synopsys, Mentor, …

- Cooperation Partners/Merge companies

- Free IP (*typically buggy, need some efforts to verify functions and get them work)
  - OpenCores: [http://www.opencores.org](http://www.opencores.org)
  - FPGA CPU News: [http://www.fpgacpu.org](http://www.fpgacpu.org)
  - ...

...
EDA Tool Markets

![Graph showing EDA tool markets from 2000 to 2007](image)

**Source:** IEK (2004/04)
SoC Challenges

- IP Resource
  - IP library, IP provider, IP quality, IP cost

- Chip Integration
  - IP cores with different manufacturer processes (logic, memory, analog, high V, …)

- Chip Design Verification
  - EDA Tools that support system verification at all or mixed design phases

- Chip Testing
  - Soft/firm/hard cores (logic, memory, analog, …) with or without test circuits, or with different testing strategies
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System-in-a-Package (SiP)

SiP concept

Packaged Chip

die

substrate

Analog

ASIC

CPU

Memory
Benefits of SiP

- SiP benefits:
  - Reduced developing schedule
  - Reduced developing cost
  - Possible mounting of different technologies
  - Increased yields enabled by smaller chip size
SiP Examples

Examples of practical SiP

Stack

Double side

Side by Side
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IC Industry Co-Operation Mode

- IDM
- Sales Channel / Service Provider
- System House (OEM/ODM)
- Design House (fabless)
- EDA Tool Company
- IP Provider
- Photo Mask/Foundry Service
- Packaging Service
- Testing Service
Taiwan IC Industry and Supporting system

EDA

Design → Foundry IDM → Assembly → Testing

Equipment

Capital & HR

Supporting Services

Transportation Custom Science Park etc.

Materials

Mask → Wafer → Chemicals → Lead Frame

Source: ITRI, DigiTimes
Role of a Design House in an IC Supply Chain

Product Development
- Market Survey
- Product Planning
- Chip Design

In-house or sub-contract

Design House

Photo Mask

Chip Manufacturing

Packaging

Wafer Testing

In-house or sub-contract

Final Test, QC

Marketing and Sales

Design House

Source: Weltrend Semiconductor, Inc
IC其實是高科技印刷出版產業

Product R&D  Mask & Wafer  Wafer CP Test  Package  Final Test  Sales & Logistics

IC設計公司  晶圓代工廠  封測公司  封測公司  封測公司  IC設計公司

Turn-key Service

作家/出版商  印刷廠  印刷廠  印刷廠  印刷廠  出版商

作品撰稿  製版 & 印刷  品管檢查  裝訂  成品檢視  配銷

Source:
IC設計業與半導體供應鍊
By Jeff Tsai
Chip Production Flow

1. Spec.
   - Market/Competitors/IP/Spec.
   - ASIC Design
   - HW/SW Design and Verification

2. EDA Tools
   - Wafer Test (Chip Probing)
   - Production Run
   - Pilot Run

3. Manufacture and Package
   - Final Test
   - Chip Verification
   - Reliability Test
   - No good
   - Ok

4. Mask Modification
   - No good
   - Chip Debugging
   - EDA Tools

5. Chip Debugging Tools

Chip Ready
Outline

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*Ref: Reuse Methodology Manual For SYSTEM-ON-A-CHIP Designs, THIRD EDITION
By Michael Keating & Pierre Bricaud
KLUWER ACADEMIC PUBLISHERS
Typical System IC Architecture

- High Speed IO
- Memory
- Processor
- Memory Controller
- Application Specific IP
- Bus Bridge
- Application Specific IP
- Interrupt Controller
- Timer
- UART/SPI/I2C
- GPIO
- High Speed Bus
- Low Speed Bus
Traditional Sequential ASIC Design Flow

1. Specification
   - Specification Define

2. System Modeling
   - Algorithm and Architecture Design

3. Circuit Design & Functional Verification
   - HDL/Schematic Circuit Design and function-simulation

4. Logical Synthesis & Timing Verification
   - Logic Synthesis and Pre-simulation

5. P & R & Physical Verification
   - Physical Design and Post-simulation

6. Prototype Build & Test
   - Prototype
Parallel System IC Design Flow

System Design and Verification

Physical
- Physical Specification: area, power, clock tree design
- Preliminary floorplan
- Updated floorplans
- Updated floorplans
- Trial placement

Timing
- Timing Specification: IO timing, clock frequency
- Block timing specification
- Block synthesis & placement
- Top-level synthesis

Hardware
- Hardware Specification
- Block selection / design
- Block verification
- Top-level HDL
- Top-level verification

Software
- Software Specification
- Application prototype development
- AP prototype testing
- Application development
- Application testing

Placement and Route -> Tapeout
Specifications

- Specification Requirements:
  - Hardware
    - Functionality
    - External interfaces to other hardware
    - Software interface (register definitions)
    - Timing
    - Performance
    - Area and power constraints
  - Software
    - Functionality
    - Timing
    - Performance
    - Hardware Interface
    - Software structure, kernel
Two Useful Specification Techniques:

- **Formal specifications:**
  The desired characteristics of a design are defined independently of any implementation. Once a formal specification is generated, format methods such as property checking can be used to prove that a specific implementation meets the specification.

- **Executable specifications:**
  An executable specification is typically an abstract model for the hardware/software been specified written in in C, C++, SystemC, HVL, Verilog, or VHDL.
System Level Design Processes

CREATE
system specification

DEVELOP
system model

SPECIFY & DEVELOP
HW architecture model

DETERMINE
HW/SW partition

REFINE & TEST
architecture model
(HW/SW co-simulation)

SPECIFY
HW block

SPECIFY & DEVELOP
Prototype SW

SPECIFY
SW

Block1 spec.

Block2 spec.
System Level Design Stages

- **Function Design**
  - Creating and verifying a functional model of the application

- **Application-driven architectural design**
  - Creating a high-level description of the platform
  - Mapping the functional application on the platform
  - Verifying the resulting architecture model
  - Finding the optimal platform

- **Platform-oriented architecture design**
  - Creating a low-level description of the platform
  - Fine-tuning the hardware architecture
<table>
<thead>
<tr>
<th>Abstraction level</th>
<th>Granularity of models</th>
<th>Simulation technology</th>
<th>Architecture exploration</th>
<th>Performance analysis</th>
</tr>
</thead>
<tbody>
<tr>
<td>Message</td>
<td>Generic HW components characterizes by external properties (universal attributes)</td>
<td>1000x speed Host-based simulator (C/C++ or systemC)</td>
<td>Application-level Very flexible</td>
<td>Platform-level (HW component = black box) Prospective(a priori)</td>
</tr>
<tr>
<td>Transaction</td>
<td>Transactional models of HW components</td>
<td>100x speed Transaction level simulator (SystemC)</td>
<td>Platform-level Less flexible</td>
<td>Component-level Confirmative (a posteriori)</td>
</tr>
<tr>
<td>Register Transfer</td>
<td>Cycle accurate models of HW components</td>
<td>1x speed RTL simulator + ISS Or FPGA-based prototyping</td>
<td>Physical level Almost not flexible</td>
<td>Detailed</td>
</tr>
</tbody>
</table>
Design Flow for Increased Chip Complexity

Front End

 RTL Design → Logical Synthesis

 Back End

 Logical Synthesis → Place & Route

 RTL

 RTL Synthesis & Prototyping → Synthesis,,Place & Route

 Netlist

 Sign off

 Sign off
Traditional Front-end Design Flow

Front-End IC Design Flow

Design Specification

- Library File
- Constraint file

RTL Design and Simulation

- Design Specification

Logic Synthesis

- static timing analysis / design rules check

- change_names / write_timing (SDF)

Pre-layout

- Gate Level Simulation

- Pre-layout

Floorplan, Placement and Route

GTL Verilog Code .vg or .VG

Front_End

1st Sign-Off
RTL Simulation Tools

- **Verilog-XL (Cadence)**: a standard sign off simulator.
- **NC-Verilog (Cadence)**: a compiled simulator, works as fast as VCS, and still maintains the sign off capabilities of Verilog-XL.
- **NC VHDL (Cadence)**: VHDL simulator.
- **NC SIM (Cadence)**: for Verilog and VHDL co-simulation.
- **VCS (Synopsis)**: a compiled simulator like NC-Verilog. This simulator is faster when it comes to RTL simulation. Few more things about this simulator are direct C kernel interface, Covermeter code coverage embedded, better integration with VERA and other Synopsys tools.
- **Scirocco (Synopsis)**: VHDL simulator.
- **Finsim (Fintronic)**: 100% compatible simulator with Verilog-XL, runs on Linux, Windows and Solaris. This is compiled simulator like VCS and NCVerilog, but slower then VCS and NCVerilog.
- **Modelsim (Mentor)**: popular and cheap simulator, has got good debugging capabilities, a nice GUI and can deal with Verilog and VHDL co-simulation. This simulator can be used for block level design and verification. But sign-off should not be done with this simulator.
- **Smash (Dolphin)**: mixed signal, Verilog, VHDL simulator
Debugging/Testbench/Rule check Tools

- **Verdi/Debussy (SprintSoft):**
  - Waveform display/probe.
  - RTL/gate-level schematic generation.
  - Finite State Machine analysis.
  - Source code tracing, …

- **Modelsim (Model Technology):**
  - Waveform display/compare.
  - Code coverage statistics.
  - Data flow tracing.
  - Memory window, …

- **VERA (Synopsys):**
  - Enables scalable and re-useable testbenches with OpenVera.

- **LEDA (Synopsys):**
  - Design rule and coding style check.
Synthesis Tools

- **Design Complier (Synopsys):**
  - the most popular logic synthesizer, bottom-up approach.

- **Ambit (Cadence):**
  - a fast logic synthesizer, top-down approach.

- **CoCentric SystemC Compiler (Synopsys):**
  - A SystemC to RTL compiler.
Synthesis Methodology

Compile Strategies

- **Bottom-up – Synopsys Design Compiler**
  - Traditional method used in building up hierarchy
  - Each module is individually synthesized
  - Uses manual time budgets or a default budget
  - May not produce optimal design
  - Prone to error in manually specified time budgets

- **Hierarchical (Top-down) – Cadence Ambit**
  - Build hierarchical design objects with constraints applied at the top-most level
  - Entire design hierarchy is optimized together
  - Only top level time budgets are required
  - Requires fewer files and produces more optimal design than with bottom-up approach
Bottom-Up synthesis Approach

- Always specify at least a default time budget!
- Time budgets are easiest with registered outputs

(Ambit) set_input_delay 2 –clock clk [find –port –input *]
set_external_delay 2 –clock clk [find –port –output *]
Hierarchical Synthesis Approach

- Hierarchical synthesis avoids inter-module time budgeting
- An entire design hierarchy is optimized together
- Sub-designs are optimized in full context of top of hierarchy
- Only top level time budgets are required

(Ambit)  do_xform_optimize_slack -time_budget
          do_optimize -time_budget
SoC Synthesis

- Recommend a bottom-up approach.
  - Each IP/macro should have its own synthesis script to ensure the right internal timing.

- Chip-level Synthesis
  - Consist only connecting the macros and resizing the output drive buffers.
Whole Chip Partitioning

- The top-levels of design hierarchy should be interconnect only
Layout Design Flow Overview

- Hierarchical Multi-million gate APR and gate level floorplan.
- Timing Driven/Power Driven/CTS (Clock Tree Synthesis) APR.
- Signal integrity (antenna/cross talk/voltage drop/electron-migration) violation analysis and removal.
- SOC integration.
- LVS/DRC/ERC physical verification.
- Scan chain re-ordering service
- Advanced 3D RC extraction (Gate Level and Transistor Level)
- SDF generate and skew report
- ECO/LVL
Clock Tree Insertion

- Small buffer -> big buffer

CLK Source

Layer 1 buffer

Layer 2 buffer

FF FF FF FF FF FF FF FF
Traditional Cell-Base Back-End Design Flow

Cell-Base Back-End IC Design Flow

- Pre-layout
- Gate Level Simulation
- Floorplan
- Placement and Route
- post-layout timing analysis / design rule check
- Physical Verification
- LVS
- APR SDF Out

Cell Library Tech File
Library Mapping File
Netlist File

GTL Verilog
Code .vg or .VG

Back_End
Traditional Cell-Base Back-End Design Flow

Logic Synthesis Optimization
Load SDF and Netlist File
APR ECO
APR SDF Out

Post APR Gate Level Simulation

Not O.K
APR ECO
APR SDF Out

O.K
Milkyway2Star ?
Yes
SDF Out
DRC/ERC/LVS
GDS II Out

No
GDS II Out

(Avanti Flow)
Layer Mapping File
Run Set File
Res TCAD File
GRD File
Skip Cell File
Star-RC Tech File
SDF Out ?
Yes
SDS Out ?
No

2nd Sign-Off
 Logic Synthesis Optimization
Load SDF and Netlist File
APR ECO
APR SDF Out

Post Layout Gate Level Simulation

Not O.K
APR ECO
APR SDF Out

O.K
Milkyway2Star

Yes

Tape Out
GDS II File
APR

- **Silicon Ensemble (Cadence)**:
  - good for interface with Cadence synthesizer.

- **SoC Encounter (Cadence)**:
  - RTL to GDSII

- **Astro/Apollo (Synopsis)**:
  - the most popular APR tool.
RC Extraction

- Hyper Extract (Cadence):

- Star-RC (Avanti/Synopsys):
  - a popular RC extraction tool

- Calibre PEX (Mentor Graphic):
Layout Verification (DRC/ERC/LVS)

- **Herculus (Avanti/Synopsys):**
  - Hierarchical, fast

- **Dracula (Cadence):**
  - Flattened, slow

- **Calibre DRC/ERC/LVS (Mentor Graphics):**
Layout Editor

- **Virtuoso (Cadence):**
- **Laker (SprintSoft):**
  - on-line rule driven & point to point routing
- **Tanner (Mentor Graphics):**
- **Enterprise (Synopsys):**
Transistor Level Verification

- **HSpice (Avanti/Synopsys):**
  - accurate but slow.

- **Star-Sim:**
  - Fast but not as accurate as HSpice.

- **P-Spice:**
  - for PC users.
Circuit Simulation Conditions

- **Operation Temperature**
  - Low (-55°C~0°C)
  - Typical (25°C)
  - High(80°C~120°C)

- **Spice Model**
  - FF/TT/SS/FS/SF
Electronic System Level (ESL) Tools

■ Purpose:
  ◆ System-level design
  ◆ HW/SW co-design
  ◆ Architecture exploration
  ◆ Virtual prototyping
  ◆ Co-simulation/co-verification

■ Requirements:
  ◆ Mixed level, mixed-language, mixed-signal simulation and debugging
  ◆ Abundant IP libraries and models
  ◆ Integrated developing environment
ESL Tools

- **CoCentric System Studio (Synopsys):**

- **Virtual Component Co-design/Incisive Function Verification Platform (Cadence):**
System-on-a-Programmable-Chip (SoPC)

- SoPC - FPGA with the following features
  - Embedded processor core
  - On-chip peripherals and memory
  - Millions of gates in FPGA logic cells
  - System level tools provided

- SoPC advantages over SoC
  - Reconfigurable
  - Fast prototyping
  - Save NRE charges
SoPC Solution

- **Xilinx – Virtex-II Pro**
  - Virtex-II Pro FPGA
  - PowerPC 405, CoreConnect bus
  - Micro Blaze controller (32-bit RISC)
  - Peripheral and memory blocks
  - EDK/ISE

- **Altera- Excalibur**
  - APEX 20KE FPGA
  - ARM 922T, AMBA bus
  - NIOS controller (16/32-bit RISC)
  - Peripheral and memory blocks
  - SoPC Builder/Quartus II
Outline

- System-on-a-Chip (SoC) Trend
- SoC Integration & Challenge
- System-in-a-Package (SIP)
- IC Industry and Chip Production Flow
- System IC Design Flow
- Chip Debugging Tools and Reliability Issues
Failure Analysis Tools

- FIB (Focused Ion Beam)
- Laser
- EMMI (EMission MIcroscope)
- Probe Station
- E-Beam
- X-Ray, SAM (Scanning Acoustic Microscope)
- Good for re-wiring digital logics.
- May not work well for analog circuits due to contact and wire resistance.
FIB Example:

- Cut and line operation
- May need to use dummy cells to modify logic circuits
- Increase or decrease the number of serially connected resistors to adjust analog parameters
EMMI Example:

Leakage
E-Beam Example:
X-Ray Example:

Wire bond .....
Reliability Testing (1)

- ESD (ElectroStatic Discharge)
  - Human-Body Mode
  - Machine Mode
  - Charged-Device Mode

- Latch Up
  - Parasitic transistors
Reliability Testing (2)

- High/Low Temperature Operating Life
- Temperature & Humidity with Bias
- High Accelerated Stress
- Pressure Cooker
- Thermal Shock
- Temperature Cycling
- High/Low Temperature Storage
- Temperature & Humidity Storage
- Temperature & Humidity Cycling
- Solderability
Summaries

- SoC is the design trend to reduce cost and system size. Some practical issues such as unified process, DFT, etc. still need to be solved.
- Difference between SoC and traditional IC design flow is addressed.
- Chip debugging tools may provide opportunity to verify circuit changes before mask modification.
- Reliability testing provides chip quality guarantee.